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L4 near4 L7	0

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<u>L7</u>	l3 near3 L6	300	<u>L7</u>
<u>L6</u>	pld or pla or (programmable adj2 logic)	36012	<u>L6</u>
<u>L5</u>	l4 near3 l3	26	<u>L5</u>
<u>L4</u>	prefetch\$	11700	<u>L4</u>
<u>L3</u>	l1 near2 l2	94932	<u>L3</u>
<u>L2</u>	(data or info or information)	5358866	<u>L2</u>
<u>L1</u>	(config or configuration)	2088185	<u>L1</u>

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## » Key

IEEE JNL IEEE Journal or Magazine

IET JNL IET Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IET CNF IET Conference Proceeding

IEEE STD IEEE Standard




- ☐ 1. **A 390-mm<sup>2</sup>, 16-bank, 1-Gb DDR SDRAM with hybrid bitline architecture**  
 Kiriha, T.; Mueller, G.; Ji, B.; Frankowsky, G.; Ross, J.M.; Terletzki, H.; Netis, D.G.;  
 Weinfurtner, O.; Hanson, D.R.; Daniel, G.; Hsu, L.L.-C.; Sotraska, D.W.; Reith, A.M.; Hug, M.A.;  
 Guay, K.P.; Selz, M.; Poechmueller, P.; Hoenigschmid, H.; Wordeman, M.R.;  
Solid-State Circuits, IEEE Journal of  
 Volume 34, Issue 11, Nov. 1999 Page(s):1580 - 1588  
 Digital Object Identifier 10.1109/4.799866  
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(628 KB\)](#) IEEE JNL  
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Thu, 15 Mar 2007, 4:45:52 PM EST

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<a href="#">#2</a>	(((((prefetch*)<in>metadata))<AND>((config <or> configuration) <and> (data <or> information)<in>metadata)))	149
<a href="#">#3</a>	((((((((prefetch*)<in>metadata))<and>((config <or> configuration) <and> (data <or> information)<in>metadata)))<AND>(pld <or> pla <or> (programmable <and> logic)<in>metadata)))	1

